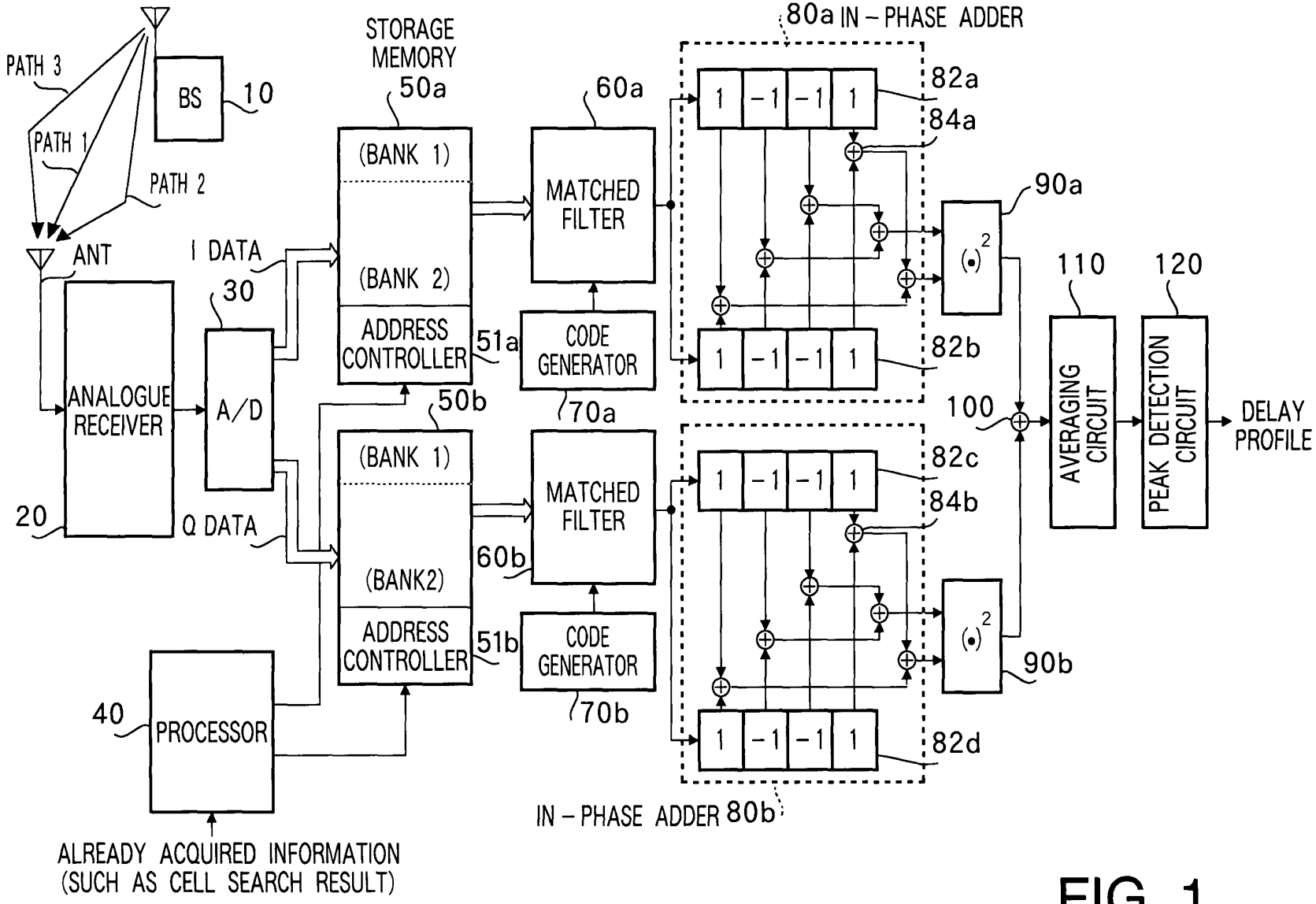
PATH 3
BS
10
PATH 1
PATH 2
ANT
I DATA
30
ANALOGUE RECEIVER
A/D
20
Q DATA
STORAGE MEMORY
50a
(BANK 1)
(BANK 2)
ADDRESS CONTROLLER
51a
50b
(BANK 1)
(BANK2)
ADDRESS CONTROLLER
51b
60a
MATCHED FILTER
CODE GENERATOR
70a
60b
MATCHED FILTER
CODE GENERATOR
70b
40
PROCESSOR
ALREADY ACQUIRED INFORMATION
(SUCH AS CELL SEARCH RESULT)
80a IN - PHASE ADDER
1 -1 -1 1
82a
84a
82b
90a
$(\bullet)^2$
82c
84b
82d
90b
IN - PHASE ADDER 80b
100
110
AVERAGING CIRCUIT
120
PEAK DETECTION CIRCUIT
DELAY PROFILE

FIG. 1

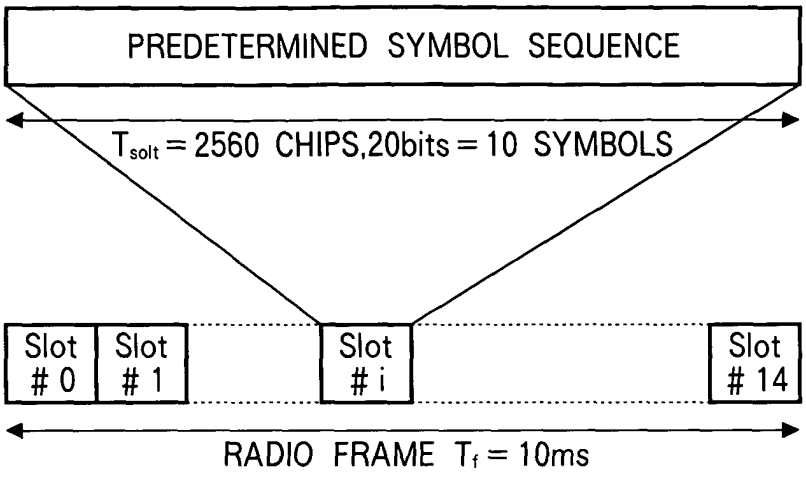
PREDETERMINED SYMBOL SEQUENCE
T_{solt} = 2560 CHIPS,20bits = 10 SYMBOLS
Slot # 0
Slot # 1
Slot # i
Slot # 14
RADIO FRAME T_f = 10ms

FIG.2A

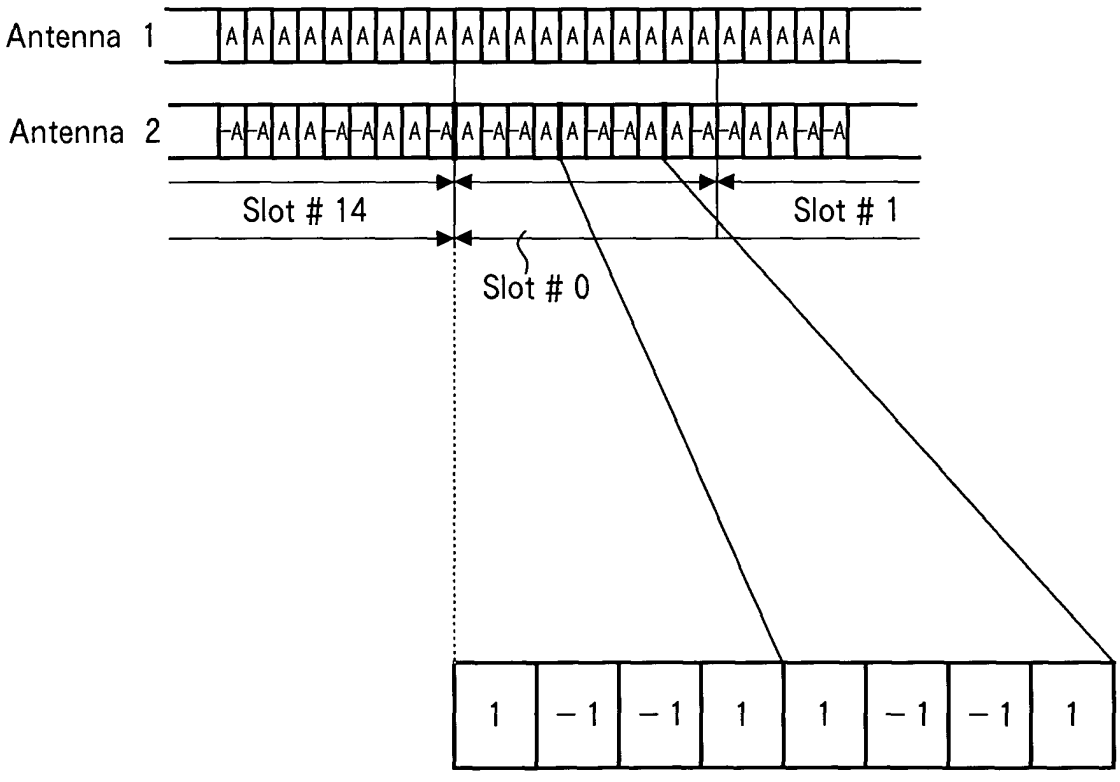
Antenna 1
Antenna 2
Slot # 14
Slot # 1
Slot # 0
1 −1 −1 1 1 −1 −1 1

FIG.2B

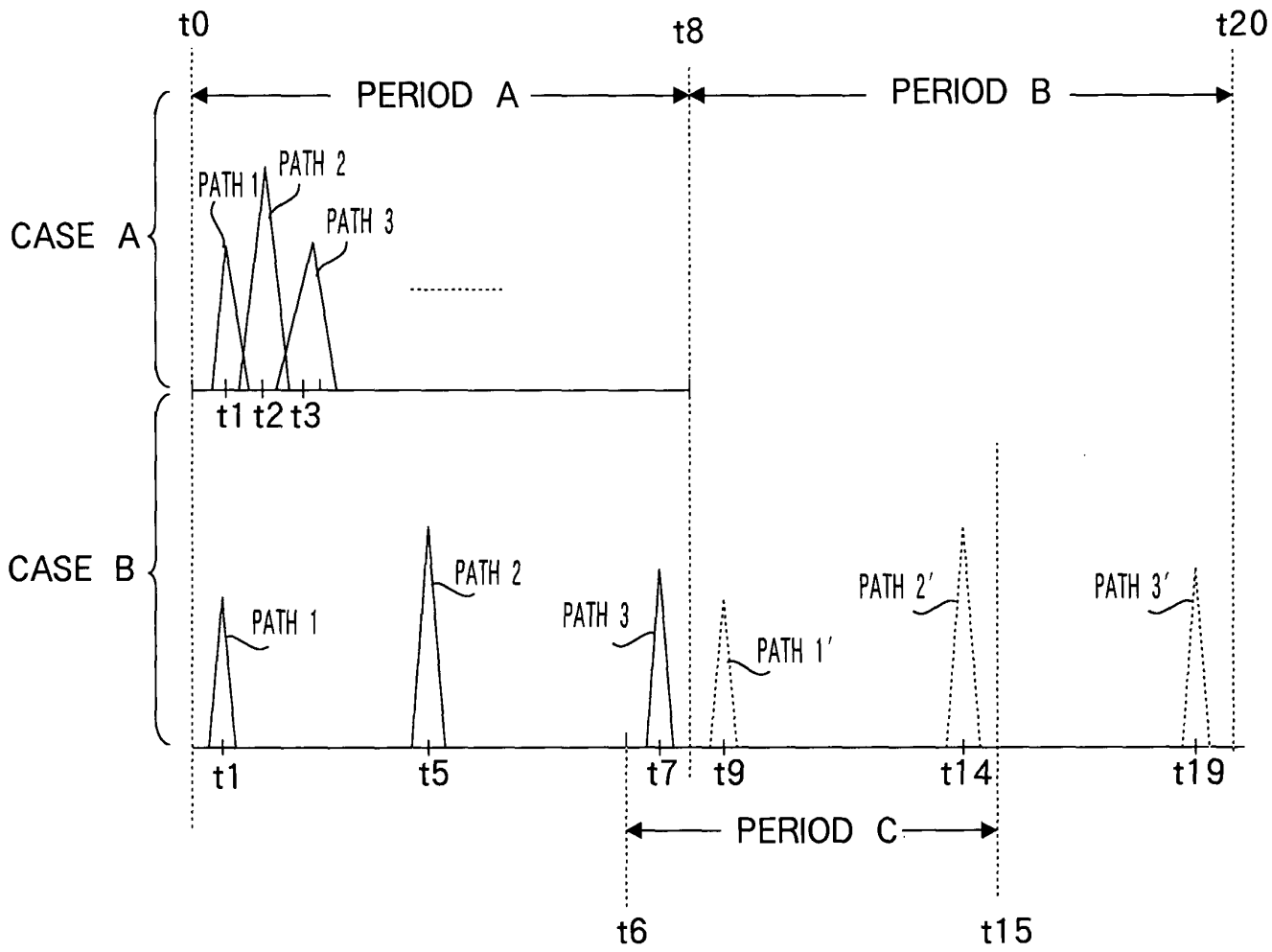
t0
t8
t20
PERIOD A
PERIOD B
CASE A
PATH 1
PATH 2
PATH 3
t1 t2 t3
CASE B
PATH 1
PATH 2
PATH 3
PATH 1'
PATH 2'
PATH 3'
t1
t5
t7
t9
t14
t19
PERIOD C
t6
t15

FIG. 3

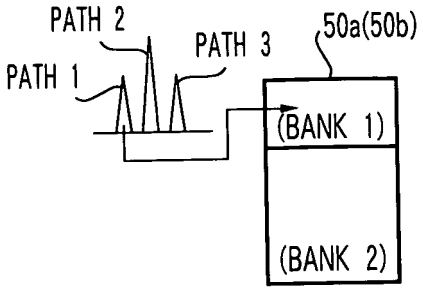

FIG.4A

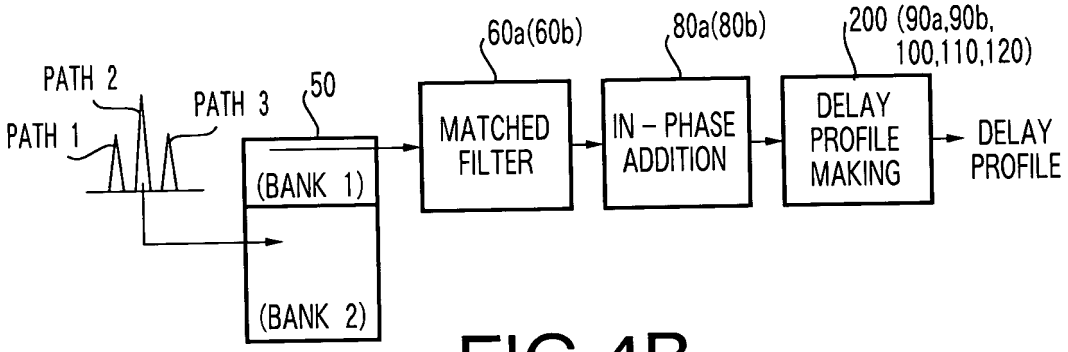

FIG.4B

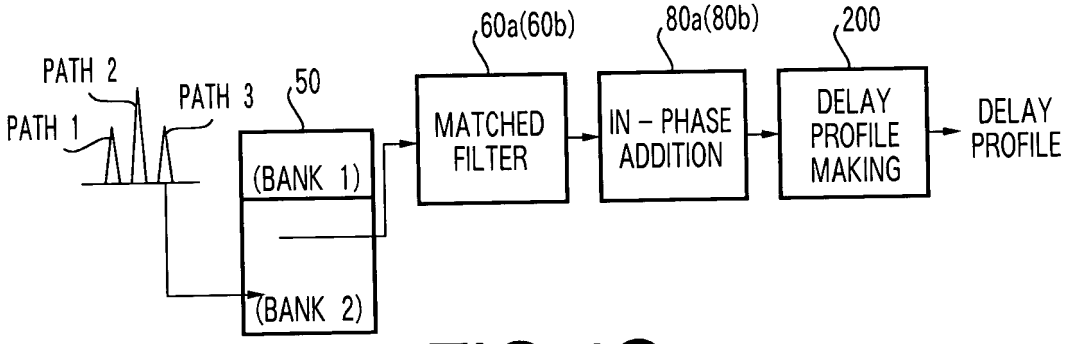

FIG.4C

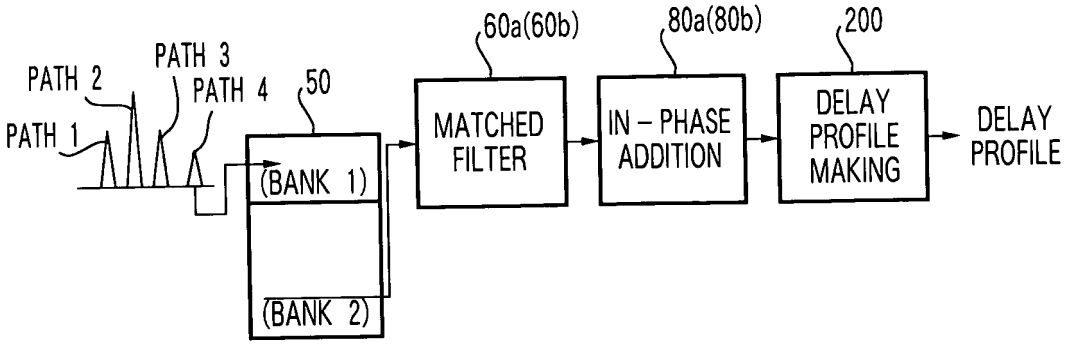

FIG.4D

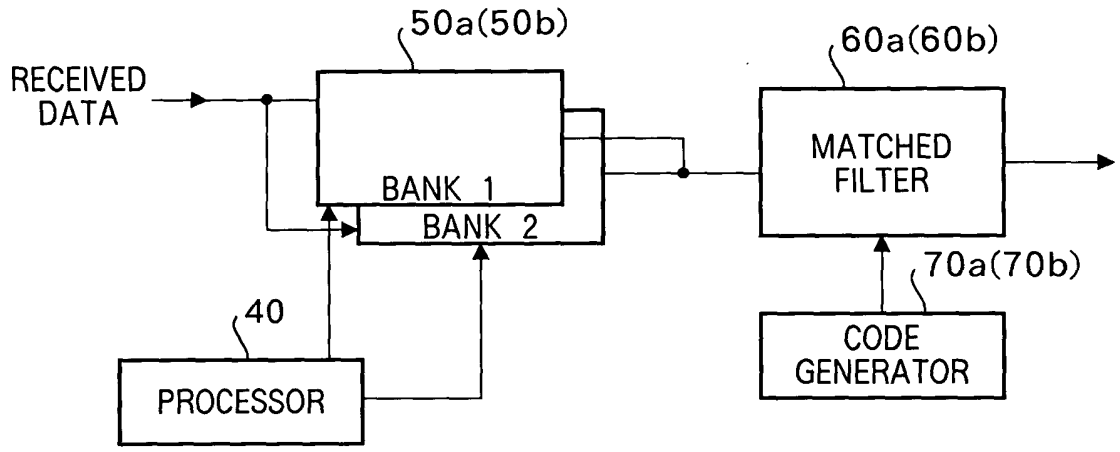
50a(50b)
60a(60b)
RECEIVED DATA
BANK 1
BANK 2
MATCHED FILTER
70a(70b)
40
CODE GENERATOR
PROCESSOR

FIG.5A

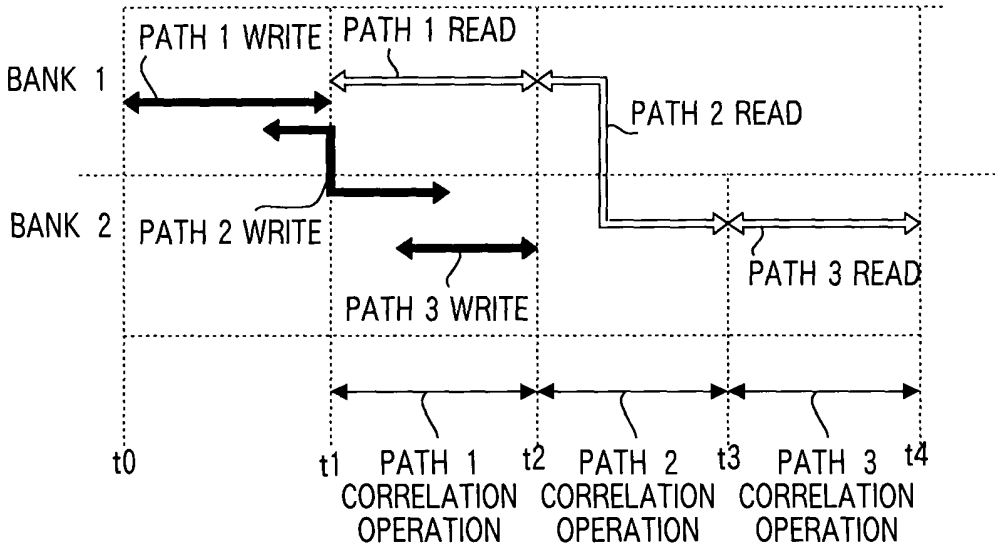
PATH 1 WRITE
PATH 1 READ
BANK 1
PATH 2 READ
BANK 2
PATH 2 WRITE
PATH 3 READ
PATH 3 WRITE
t0
t1
PATH 1 CORRELATION OPERATION
t2
PATH 2 CORRELATION OPERATION
t3
PATH 3 CORRELATION OPERATION
t4

FIG.5B

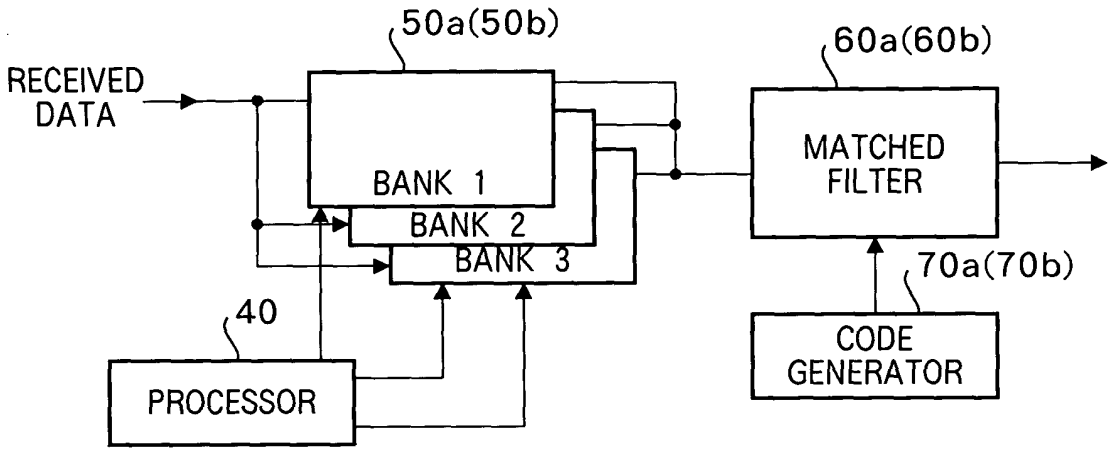
50a(50b)
60a(60b)
RECEIVED DATA
BANK 1
BANK 2
BANK 3
MATCHED FILTER
70a(70b)
40
CODE GENERATOR
PROCESSOR

FIG.6A

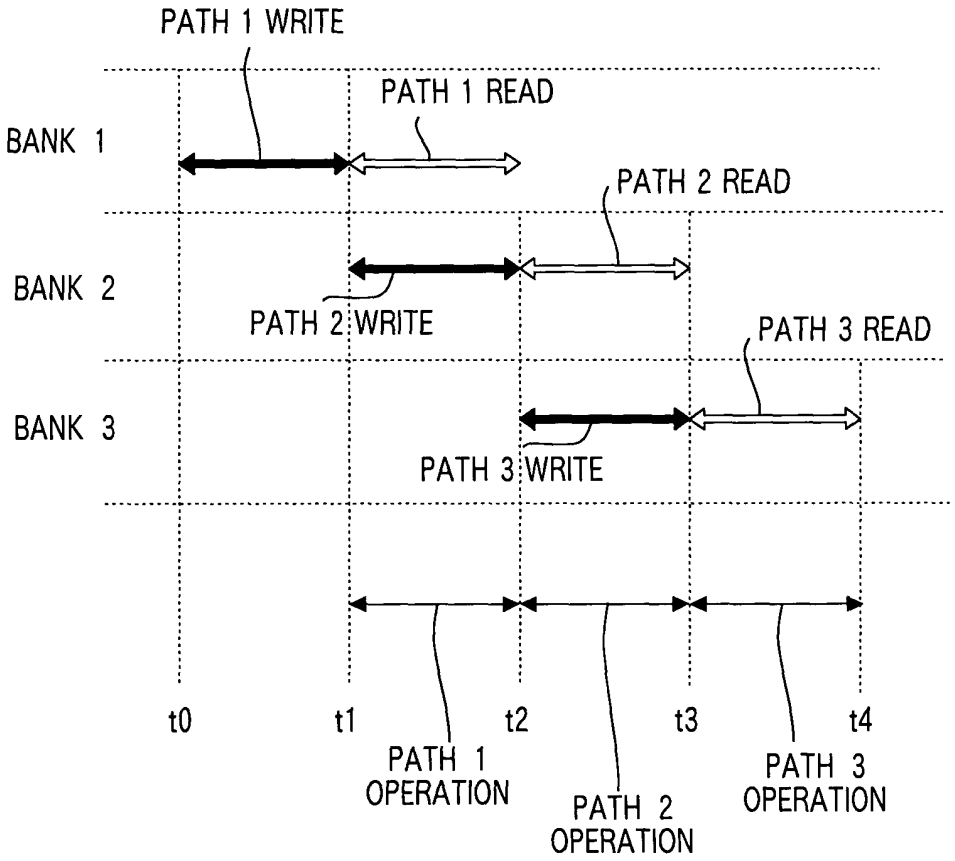
PATH 1 WRITE
PATH 1 READ
BANK 1
PATH 2 READ
BANK 2
PATH 2 WRITE
PATH 3 READ
BANK 3
PATH 3 WRITE
t0
t1
t2
t3
t4
PATH 1 OPERATION
PATH 2 OPERATION
PATH 3 OPERATION

FIG.6B

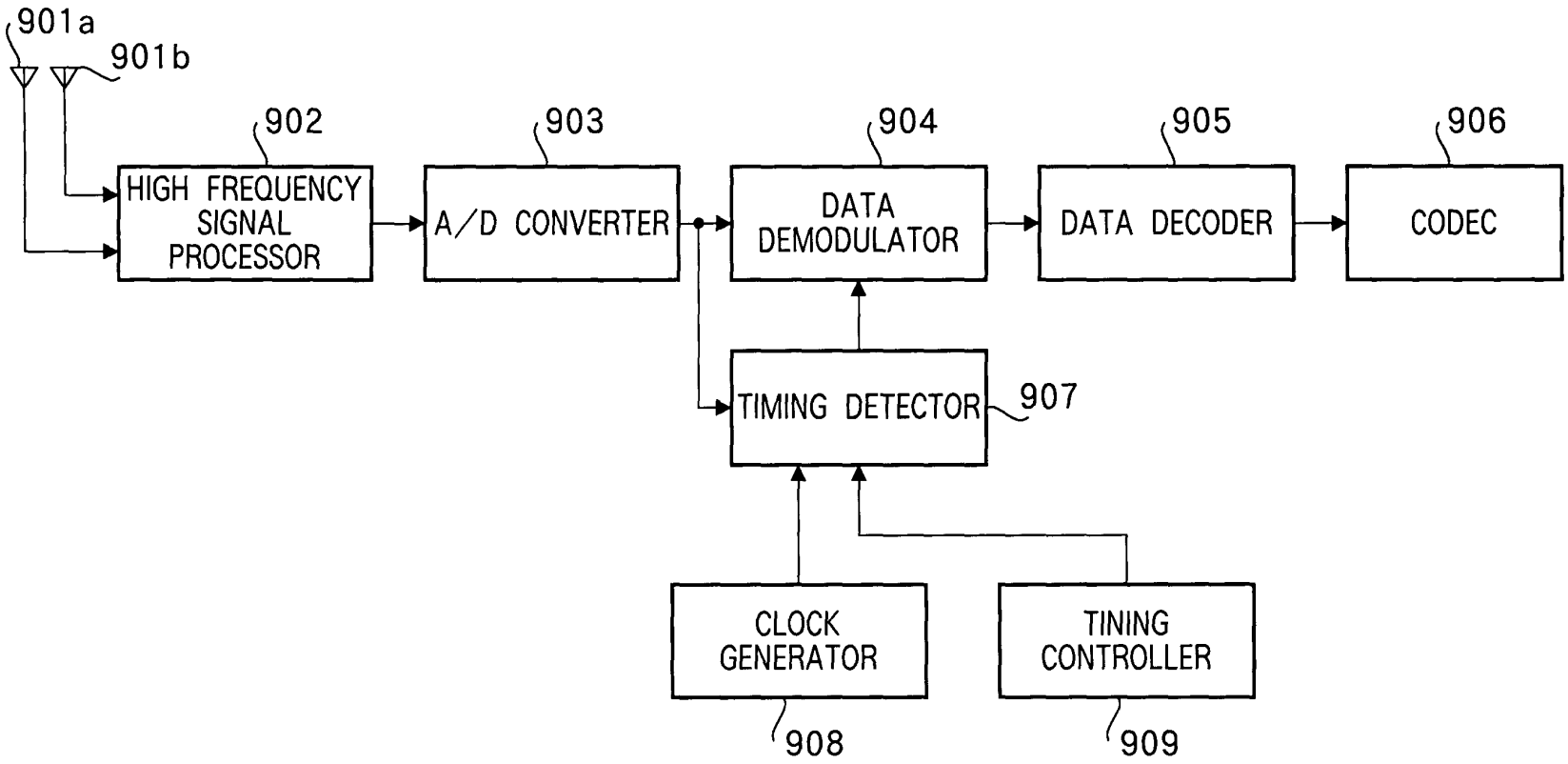
901a
901b
902
903
904
905
906
HIGH FREQUENCY SIGNAL PROCESSOR
A/D CONVERTER
DATA DEMODULATOR
DATA DECODER
CODEC
TIMING DETECTOR
907
CLOCK GENERATOR
TINING CONTROLLER
908
909

FIG. 7

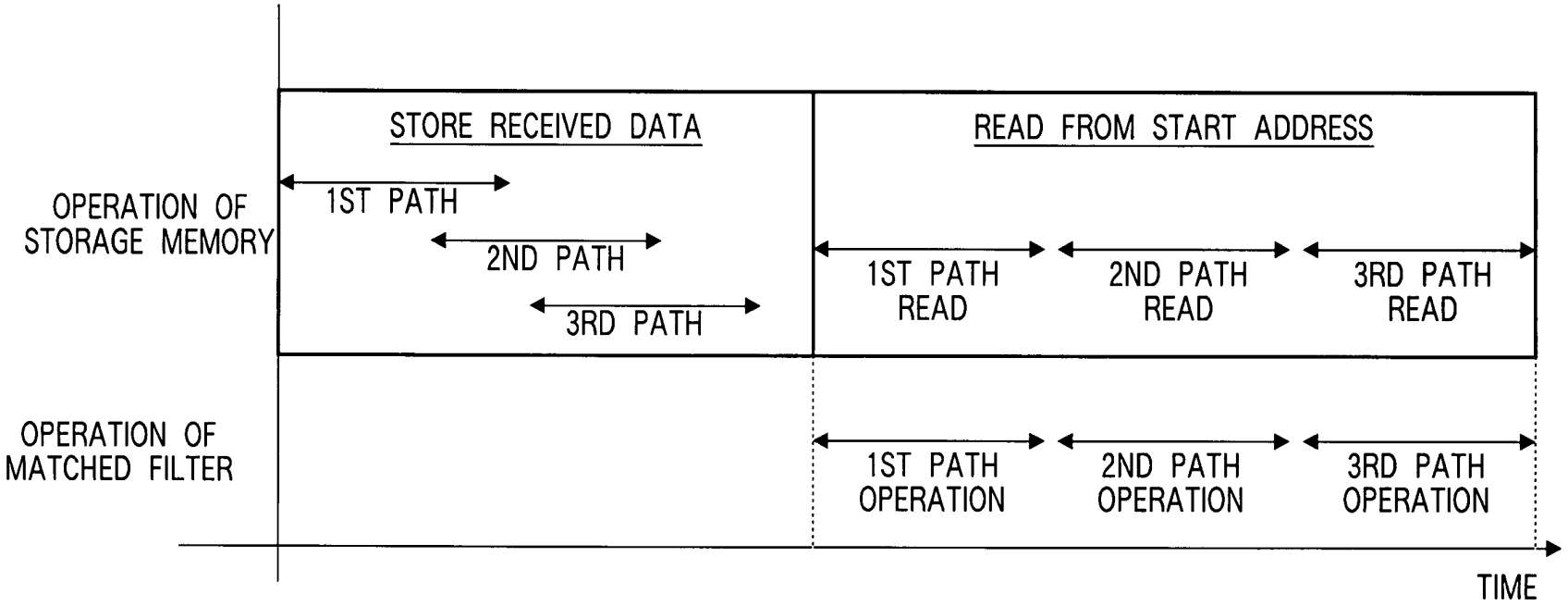
STORE RECEIVED DATA
READ FROM START ADDRESS
OPERATION OF STORAGE MEMORY
1ST PATH
2ND PATH
3RD PATH
1ST PATH READ
2ND PATH READ
3RD PATH READ
OPERATION OF MATCHED FILTER
1ST PATH OPERATION
2ND PATH OPERATION
3RD PATH OPERATION
TIME

FIG. 8